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Department of Electronics & Communication Engineering

Lab Manual

147351 DIGITAL ELECTRONICS

Class: 2nd yr, 3rd sem

SYLLABUS

1. Design and implementation of Adders and Subtractors using logic gates.
2. Design and implementation of code converters using logic gates
 - (i) BCD to excess-3 code and vice versa
 - (ii) Binary to gray and vice-versa
3. Design and implementation of 4 bit binary Adder/ subtractor and BCD adder using IC 7483
4. Design and implementation of 2 Bit Magnitude Comparator using logic gates 8 Bit Magnitude Comparator using IC 7485
5. Design and implementation of 16 bit odd/even parity checker generator using IC74180.
6. Design and implementation of Multiplexer and De-multiplexer using logic gates and study of IC74150 and IC 74154
7. Design and implementation of encoder and decoder using logic gates and study of IC7445 and IC74147
8. Construction and verification of 4 bit ripple counter and Mod-10 / Mod-12 Ripple counters
9. Design and implementation of 3-bit synchronous up/down counter
10. Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip-flops.
11. Design of experiments 1, 6, 8 and 10 using Verilog Hardware Description Language (Verilog HDL).



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